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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/557,088	04/21/2000	Hiroshi Sonabe	HYAE:097	6278

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EXAMINER

DOOLEY, MATTHEW C

ART UNIT	PAPER NUMBER
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2133

DATE MAILED: 04/11/2003

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Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/557,088

Applicant(s)

SONABE, HIROSHI

Examiner

Matthew C. Dooley

Art Unit

2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 21 April 2000.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-4 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 April 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☒ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Endoh et al., U.S. 5,485,094, in view of Ferguson et al., U.S. 6,202,181.

As per claim 1:

Endoh teaches to a semiconductor inspection method that includes obtaining input logical values such that adjacent lines have complimentary logical values (Fig.1: 10, 11: P3), as well as monitoring the output of a logical circuit that receives the input values and comparing the monitored output values with a set of expected data values (Fig.3: 35) for determination of short circuit occurrences between device lines (Col.1: 62-67). However, not taught by Endoh is that specific lines should be extracted from the tested devices, wherein the aforementioned lines are adjacent to one another. Ferguson teaches to a method of short circuit determination testing in semiconductor circuits wherein adjacent lines are extracted for testing purposes (Col.10: 17-24). It would have been obvious for one of ordinary skill in the art at the time of the invention to make use of the method of adjacent line testing taught by Ferguson with the testing method of Endoh because the method of Ferguson allows for fewer lines to have to be tested, thus leading to faster device testing (Col.10: 23-24). Endoh clearly and particularly demonstrates motivation

Art Unit: 2133

for rapid testing and minimum pattern selection in the testing methodology (Col.1: 62-67), and thus, one skilled in the art would be motivated to combine the testing methodologies of the aforementioned references for faster circuit testing.

As per claim 2:

Claim 2 is similar in scope to that of claim 1, with the additional limitation of the extraction of data lines must be made when the distance between the lines is equal to or less than a threshold. Ferguson teaches to this additional limitation (Col. 10: 21-24). The remaining limitations are rejected using analogous reasoning to that used in the rejection of claim 1 above.

As per claim 3:

Claim 3 is analogous to claim 1 and as such, is rejected using analogous reasoning to that used in the rejection of claim 1 above.

As per claim 4:

Claim 4 is analogous in scope to claim 2 and as such, is rejected using analogous reasoning to that used in the rejection of claim 1 above.

3. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Endoh et al., U.S. 5,485,094, in view of Parker et al., U.S. 5,513,188.

As per claim 1:

Endoh teaches to a semiconductor inspection method that includes obtaining input logical values such that adjacent lines have complimentary logical values (Fig.1: 10, 11: P3), as well as monitoring the output of a logical circuit that receives the input values and

Art Unit: 2133

comparing the monitored output values with a set of expected data values (Fig.3: 35) for determination of short circuit occurrences between device lines (Col.1: 62-67). However, not taught by Endoh is that specific lines should be extracted from the tested devices, wherein the aforementioned lines are adjacent to one another. Parker teaches to a method of short circuit determination testing in semiconductor circuits wherein adjacent lines are extracted for testing purposes (Fig.6; Fig.8: 802; Col.8: 4-14, 24-43). It would have been obvious for one of ordinary skill in the art at the time of the invention to make use of the method of adjacent line testing taught by Parker with the testing method of Endoh because the method of Parker allows simplification of testing because fewer lines to have to be tested, thus leading to faster device testing (Col.6: 16-20). Endoh clearly and particularly demonstrates motivation for rapid testing and minimum pattern selection in the testing methodology (Col.1: 62-67), and thus, one skilled in the art would be motivated to combine the testing methodologies of the aforementioned references for faster circuit testing.

As per claim 2:

Claim 2 is similar in scope to that of claim 1, with the additional limitation of the extraction of data lines must be made when the distance between the lines is equal to or less than a threshold. Parker teaches to this additional limitation (Fig.6; Col.8: 4-14, 24-43). The remaining limitations are rejected using analogous reasoning to that used in the rejection of claim 1 above.

As per claim 3:

Art Unit: 2133

Claim 3 is analogous to claim 1 and as such, is rejected using analogous reasoning to that used in the rejection of claim 1 above.

As per claim 4:

Claim 4 is analogous in scope to claim 2 and as such, is rejected using analogous reasoning to that used in the rejection of claim 1 above.

***Conclusion***

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Chang et al. U.S. 6,370,594: (Fig. 5)

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Dooley whose telephone number is (703) 306-5538. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.



Matthew Dooley  
Examiner AU 2133  
April 3, 2003



ALBERT DECADY  
SUPERVISORY PATENT EXAMINER  
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